QMP6990 Digital Waterproof Barometric Pressure Sensor

QMP6990 is a digital barometric pressure sensor especially designed for applications requiring highly-precision pressure measurement like quadcopter altitude control and portable navigation device. It is both a pressure and temperature sensor housed in a compact 2.0×2.0×0.95 mm3 package. The pressure sensor is based on the industry-recognized piezo-resistive technology featuring long-term stability and EMC robustness. A high-performance 24-bit ADC provides pressure resolution up to 0.015Pa, and temperature resolution up to 0.1℃. The pressure sensor has a wide operating range from 300 to 1250hPa that covers all surface elevations on earth.

QMP6990 can detect absolute barometric pressure with highly accuracy for applications like quadcopter altitude control. The maximum altitude resolution can be up to less than 5cm. Several operation options further offer large window for user optimization on the power consumption, resolution and filter performance.

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FEATURES

- Operation range:
  - Pressure: 300~1250hPa (Absolute)
  - Temperature: -40~+85℃
- Built-in 24-bit ADC:
  - Pressure resolution: 0.015Pa (1/64 Pa)
  - Temperature resolution: 0.1 ℃
  - FIFO 576 bytes
  - Interrupt: Data ready, FIFO status
- Digital interface:
  - I2C: standard and fast modes
  - SPI: 3-/4-wire, up to 10MHz clock
- Supply voltage:
  - VDD: +1.71V ~ +3.3V
  - VID: +1.71V ~ +3.3V
- Power consumption:
  - Standby ~ 1.2uA
- RoHS-compliance package:
  - 10-pin LGA with metal lid
  - Footprint: 2.0 × 2.0 mm²
  - Height: 0.95 mm.

CONTENTS

1 NTERNAL SCHEMATIC DIAGRAM

1.1 Internal Schematic Diagram

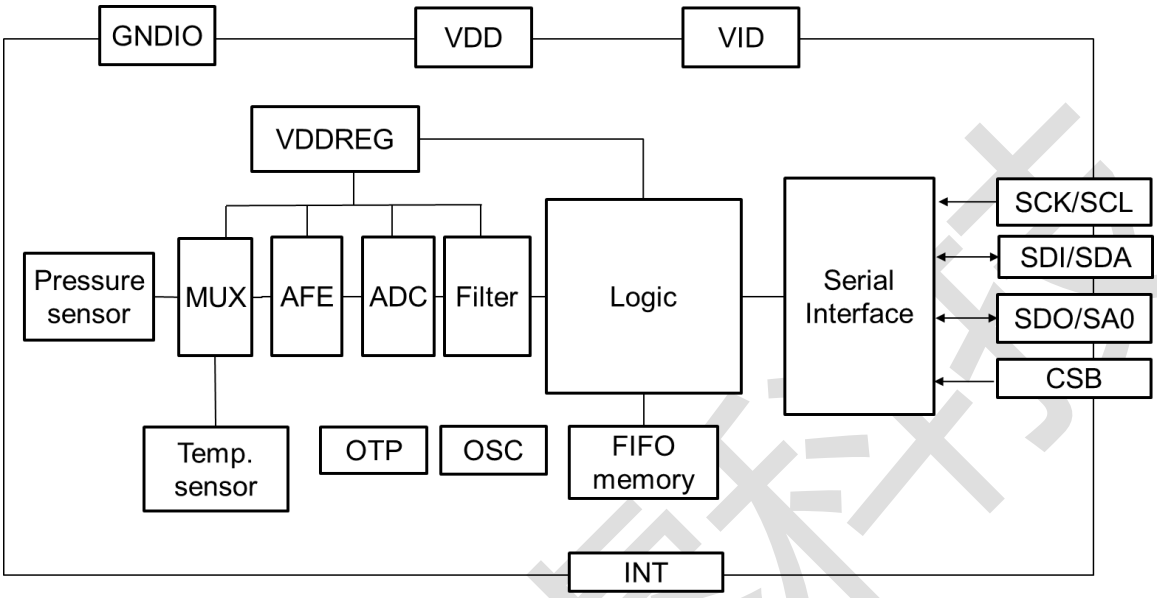


Figure 1. Block Diagram

2 SPECIFICATIONS

2.1 Product Specifications

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power supply voltage Main Condition	VDD, VDDIO		1.7	1.8	1.98	V
Power supply voltage Main Condition	VDD, VDDIO		2.97	3.3	3.63	V
Temperature range	Ta		-40	25	+85	°C
Pressure range	P		300	—	1250	hPa
Operation current	POSR=X4 POSR=X8 POSR=X16 POSR= X32 POSR= X64	VDD = 1.8V 20Hz TOSR=X1 P+T conversion	—	47 82 150 288 564	—	uA
Standby current	IDDSD	VDD = VDDIO = 1.8V	—	1.2	—	uA

Relative accuracy pressure	PREL	700 to 1100 hPa 25°C to 40°C 10kPa Step	—	±0.06	—	hPa
Absolute accuracy pressure*1	PABS	300 to 1100 hPa 0°C to 65°C VDD=1.8V	—	±0.5	—	hPa
Offset temperature coefficient*2	TCO	1000 hPa 25°C to 40°C	—	±0. 75	—	Pa/K
Noise in pressure		in pressure lowest bandwidth, highest resolution, with low pass filter enabled	—	0.1	—	Pa RMS
Absolute accuracy temperature	TABS	0~65°C	—	±1.5	—	°C
Solder drift*3			—	±1		hPa
Long term stability (12 months)		0°C to 65°C	—	±0.5	—	hPa

*1 95% samples keep the absolute accuracy at typical value. The accuracy is measured based on dedicated chamber and pressure meter.

*2 The TCO is tested by sensor mounted on evaluation board and heated from 25 to 40℃.

*3 The solder drift typical value is tested at 24 hours later after reflow. If tested at 6 hours after reflow, 75% samples are smaller than 1 hPa.

*4 Sensor calibrated at VDD = 1.8V and VDDIO = 1.8V condition.

2.2 Absolute Maximum Ratings

Table 2. Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit
Power supply voltage	VDD, VDDIO	-0.3	3.6	V
Signal input voltage	VIS	-0.3	3.6	V
Pressure	PMAX	0	1	MPa
Storage temperature	STG	-40	+85	°C
ESD	HBM	—	±2	kV
	CDM	—	500	V
	MM	—	200	V
	Latch Up	—	100	mA

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

3 PACKAGE PIN CONFIGURATIONS

3.1 PIN definition

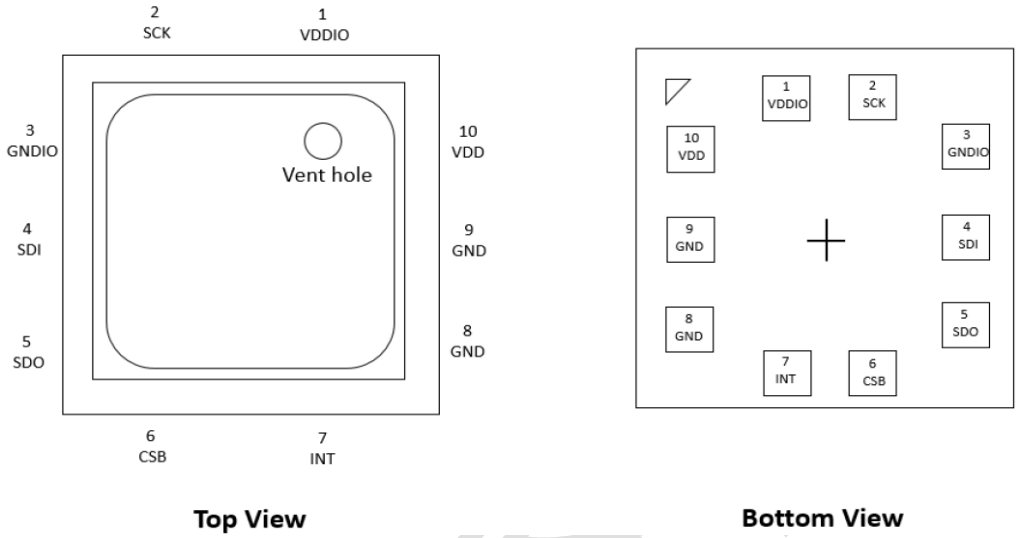


Figure 2. Pin definition, upper view, and bottom view

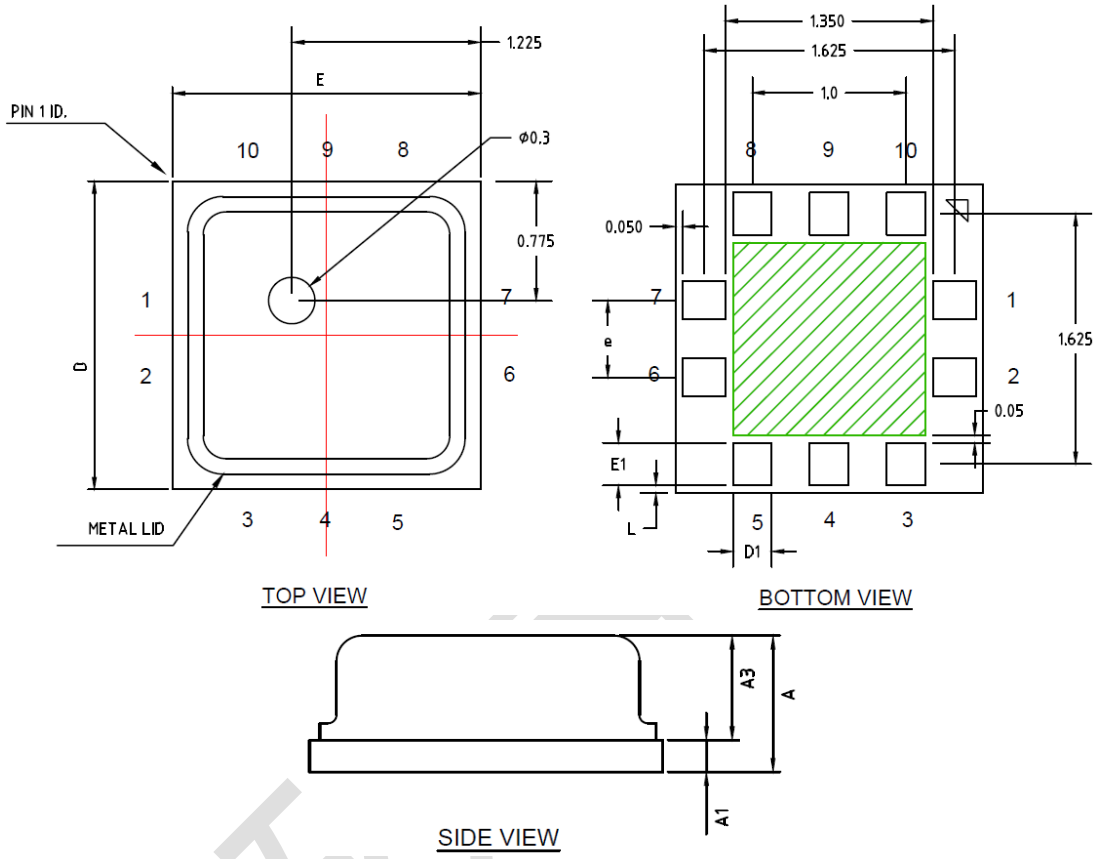
Table 3. Pin Configurations

Pin#	Name	Description
1	VDDIO	Digital interface power supply in
2	SCL/SCK	Serial clock input
3	GNDIO	Ground
4	SDA/SDI/ SDIO	Serial data input -Serial Data (I2C, Open-Drain). -Serial Data Input (SPI 4-Wire). -Serial Data Input and Output (SPI 3-Wire).
5	SA0/SDO	Serial data output -I2C slave address selection pin, 0 for 0x3A, 1 for 0x3B -Serial Data Output (SPI 4-Wire)/ NC (SPI 3-Wire).
6	CSB	I2C/SPI mode select 0' for SPI mode. '1' or floating for I2C mode.
7	INT	Interrupt
8	GND	Ground
9	GND	Ground
10	VDD	Core circuit power supply in

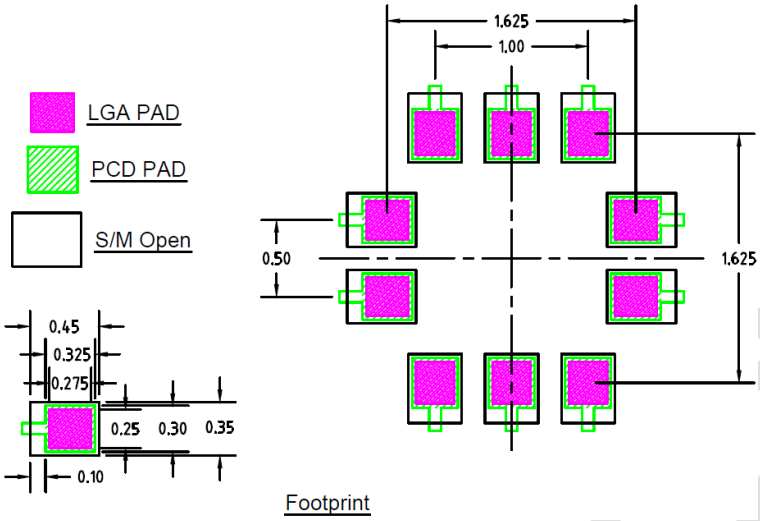
3.2 Package Type

LGA

3.3 Package Size



SYMBOL	DIMENSION (mm)		
	MIN.	NOM.	MAX.
A	0.75	0.85	0.95
A1	0.12	0.15	0.18
A3	0.63	0.70	0.77
D	1.95	2.0	2.05
D1	0.20	0.25	0.30
E	1.95	2.0	2.05
E1	0.225	0.275	0.325
e	---	0.50 REF.	---
L	---	0.05 REF.	---



Recommended PCB Foot Print Layout

Figure 3. Package Size

RoHS Compliance

QMP LGA with metal lid packaged sensors are compliant with Restrictions on Hazardous Substances (RoHS), having halide-free molding compound (green) and lead-free terminations. Reflow profiles applicable to those processes can be used successfully for soldering the devices.

Moisture Sensitivity Level and Device Storage

QMP6990 package MSL rating is Level 1 according to IPC/JEDEC standards J-STD-020D.

- ✓ The soldering process and moisture can lead to absolute pressure shift.
- ✓ The device need to be recalibrated the absolute pressure shift after soldering process. QMP6990 keeps the same condition after the offset adjustment.
- ✓ Manual unsoldering can lead to further offset shift if the soldering temperature and soldering time is above 260°C and 40 secs.
- ✓ Avoid to contact the liquids or small particles.

4 BUS INTERFACE

4.1 I²C Bus interface

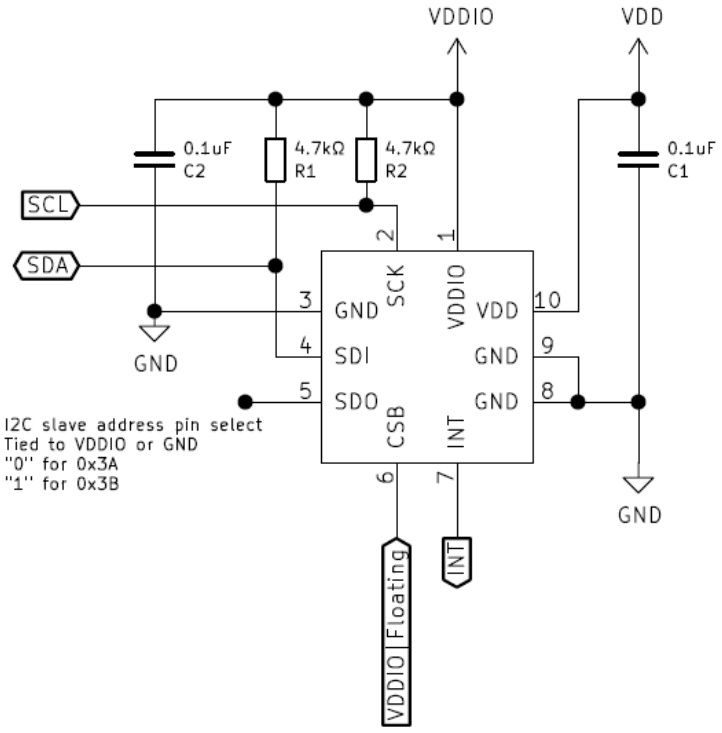


Figure 4: QMP6990 I2C Connection Example

4.2 SPI Bus interface

SPI 4-wire Interface

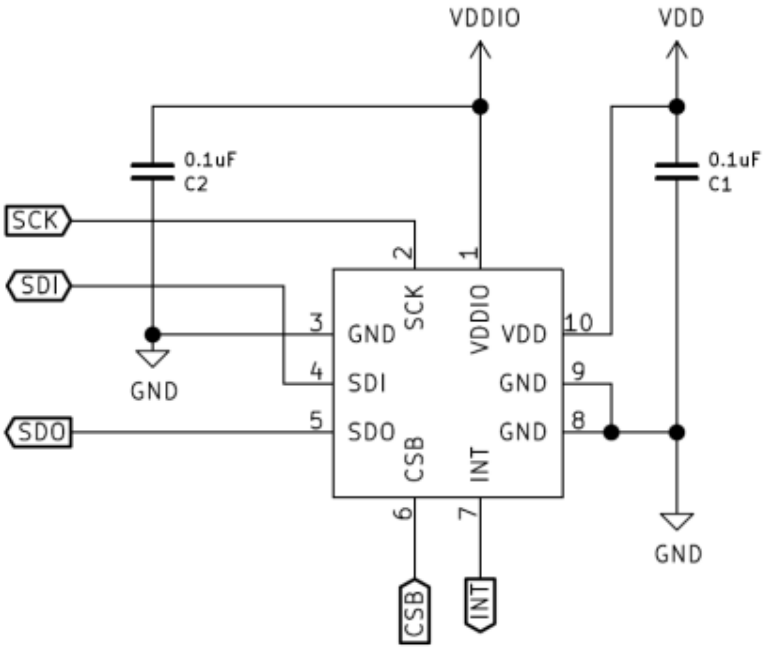


Figure 5: QMP6990 SPI 4-Wire Connection Example

SPI 3-wire Interface

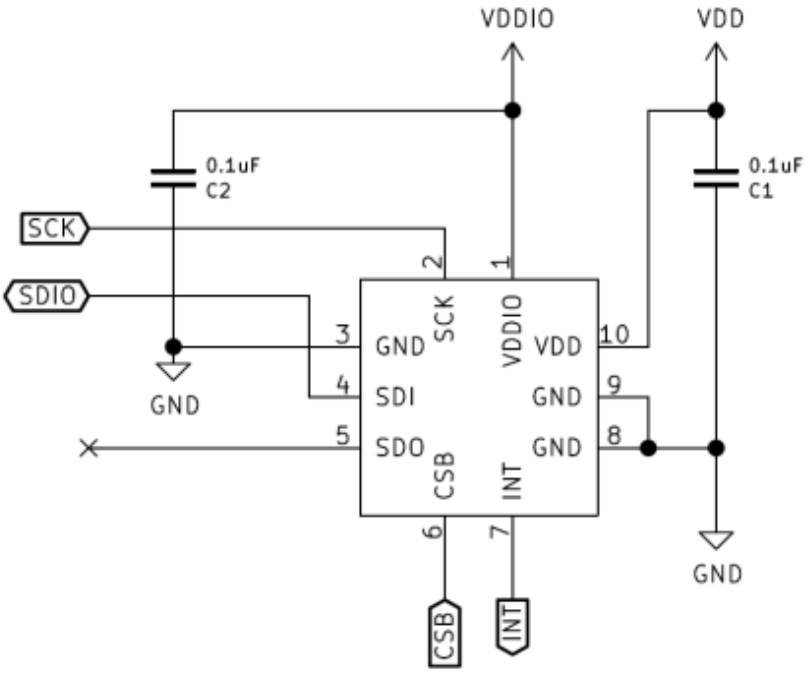


Figure 6: QMP6990 SPI 3-Wire Connection Example

5. FUNCTIONAL DESCRIPTION

5.1 Power Management

The QMP6990 has two power supply pins, VDD and VDDIO. VDD is the main power supply for all internal voltage regulator blocks. VDDIO is used to power the digital interface. All voltage and ground supplies must be provided for the IC to function properly.

After the power-on sequence, the built-in power-on reset generator is activated, resetting the logic circuits and the registers to default states.

5.2 Operation Mode

The QMP6990 has three different power modes, normal mode, force mode, and sleep mode. After power-on reset, the sensor enters sleep mode, the user can use the PWR_MODE[1:0] bits in control register PWR_CTRL(0x1B) to switch to normal mode or force mode for measurement.

PWR_MODE[4:0]	Mode
2'b00	Sleep mode
2'b01	Force mode
2'b10	reserved
2'b11	Normal mode

If the device is currently performing a measurement, the execution of the mode switch command will be delayed until the end of the currently running measurement period and further mode change commands will be ignored. The mode transition diagram is shown below.

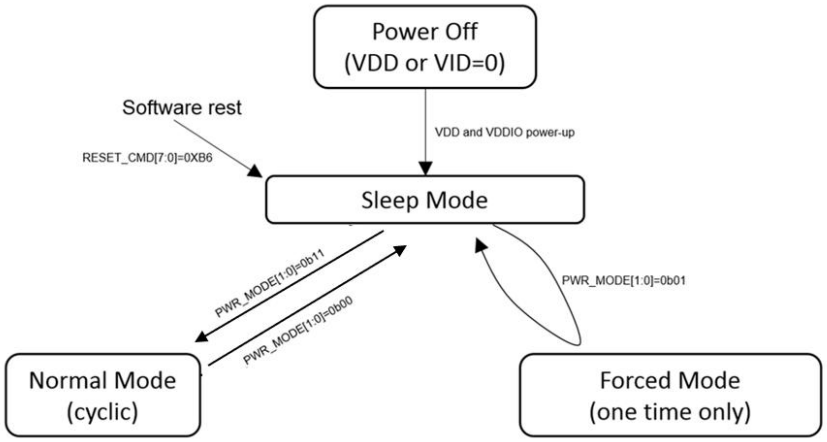


Figure 7: Mode transition diagram

Sleep mode

In sleep mode, whole analog and oscillator are power-down except for the low-power clock. No data acquisition is performed to minimize power consumption. In the sleep mode, the output data doesn't clear or update, but keeps the last value before entering sleep mode.

Normal mode

In normal mode, all functions are available and data acquisition is performed continuously and switch automatically between a measuring period and a sleep period. The final measurement result is available from the data register and updated with the measurement rate which can be set by ODR_SEL[5:0] in the register ODR(0x1D). Using an IIR filter in normal mode can filter out short-term interference well.

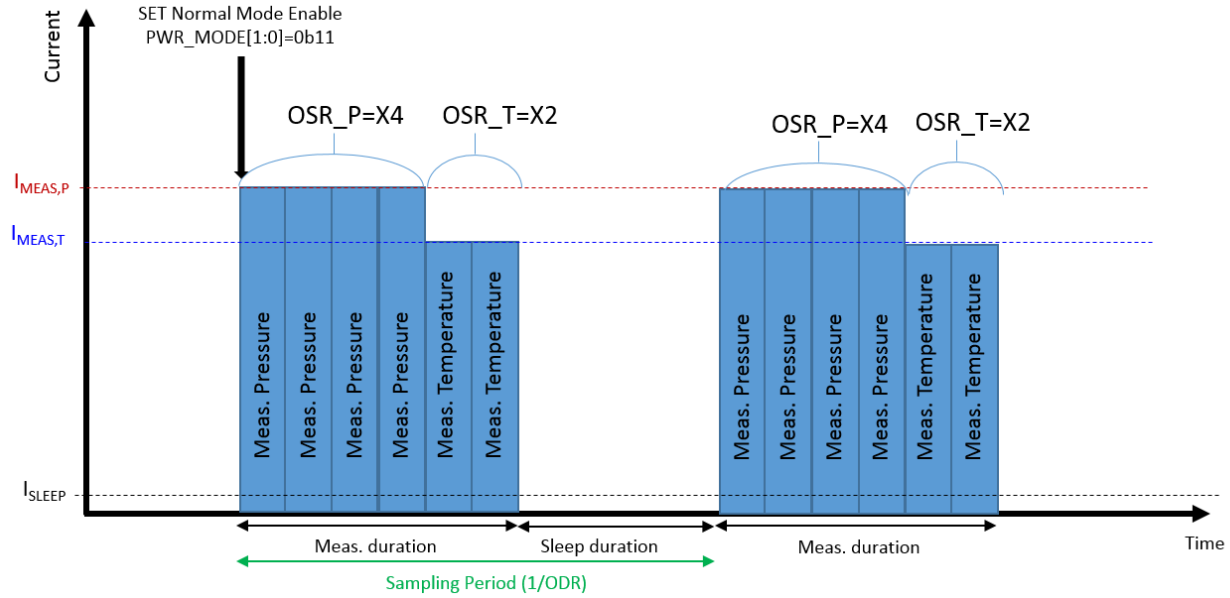


Figure 8: Normal mode timing diagram

Force mode

In forced mode, only one measurement is performed based on selected oversampling and filter options. After the measurement is completed, the sensor returns to sleep mode and the measurement results is available from the data register. Force mode needs to be set again to the next measurement.

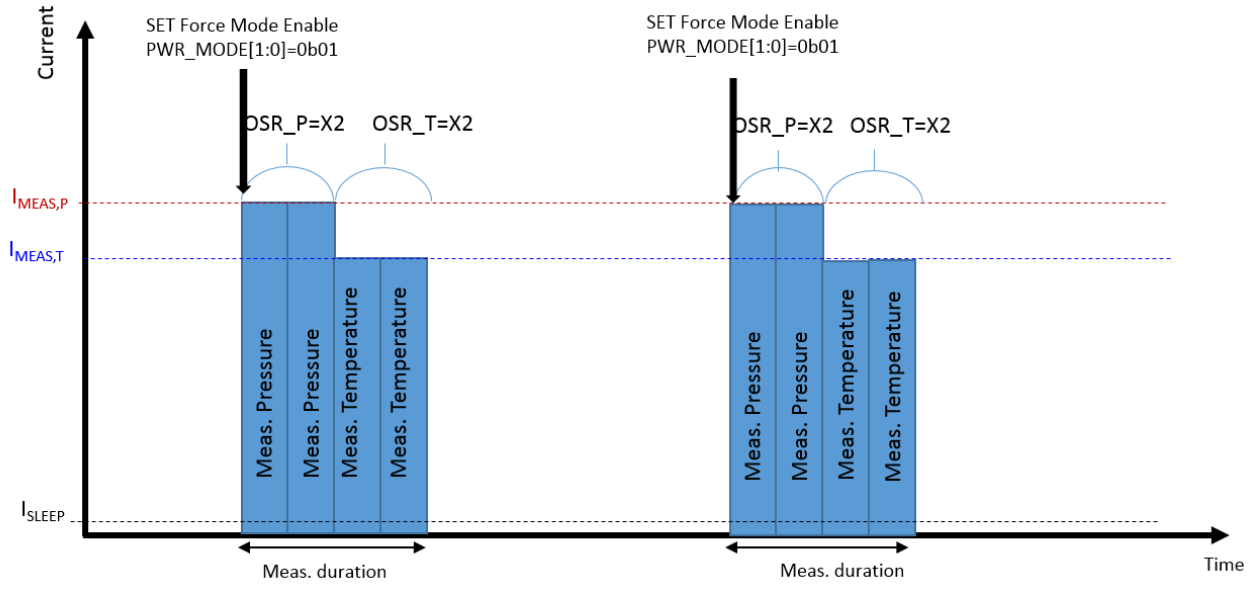


Figure 9: Force mode timing diagram

Reset Function

Reset of QMP6990 is described as below:

✓ Soft reset: Set RESET register (7Eh) to 0xB6 will trigger the device soft reset by resetting all registers to default value, and set IC to default state.

5.3 FIFO

The QMP6990 features an integrated FIFO memory capable of storing up to 576 bytes, which allows collecting 96 samples of 24 bits for the pressure and temperature data at the same point on the timeline.

FIFO use allows consistent power saving for the system, it can wake up only when needed and burst the data out from the FIFO. The FIFO buffer can work according to three different modes: Bypass mode, FIFO mode, Stream mode.

FIFO_EN bit	FIFO_MODE bit	FIFO mode selection
0	0 or 1	Bypass Mode
1	0	Stream Mode
1	1	FIFO Mode

Bypass mode

In bypass mode, only the current sensor data can be read out from the FIFO address. Essentially, the FIFO behaves like the stream mode with a depth of 1. If user reads the data from FIFO buffer, it can be guaranteed that the pressure data and temperature data are from the same timestamp.

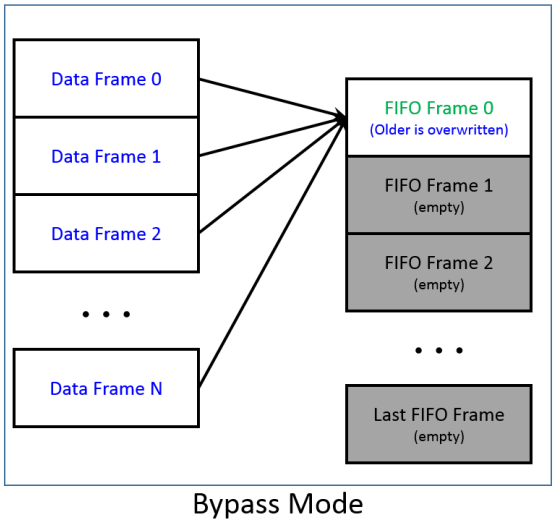


Figure 10: Bypass mode

FIFO mode

In FIFO mode, the data of the selected measurement type is continuously stored in the buffer until the unread data reaches 576 bytes. When the FIFO is full, the data collection is stopped, and new data is ignored. If FIFO mode is enabled, a watermark interrupt will be triggered when the buffer is filled to a configurable level. Once the buffer is full, a FIFO-full interrupt also generates if it has been enabled.

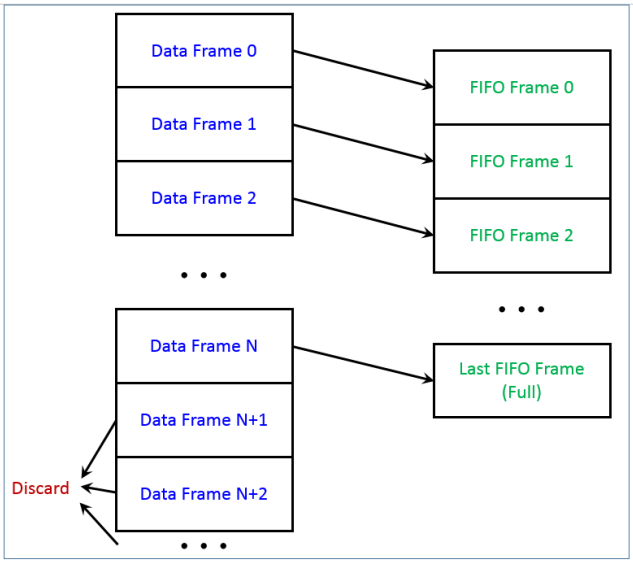


Figure 11: FIFO mode

Stream mode

In stream mode, the data of the selected measurement type is continuously updated in the buffer. When the buffer is full, as new data arrives the oldest data is discarded and overwritten by the newer. If stream mode enabled, a watermark interrupt is triggered when the buffer is filled to a configurable level. Once the buffer is full, a FIFO-full interrupt generates if it has been enabled.

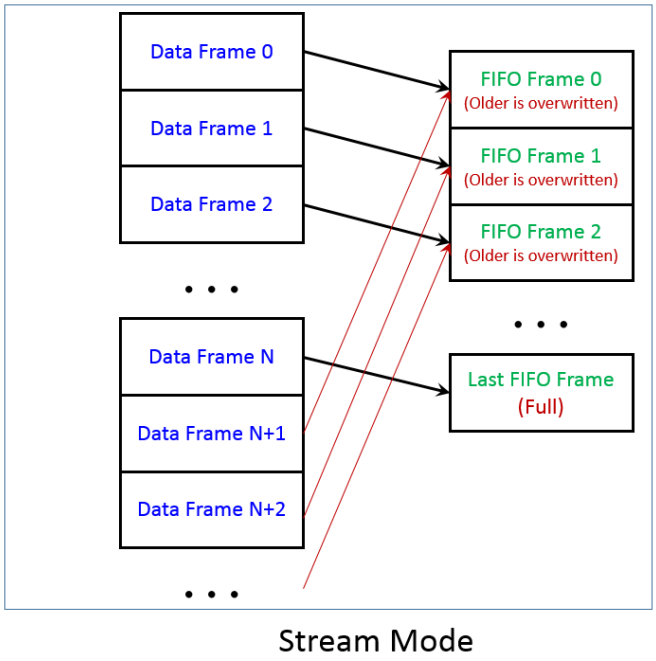


Figure 12: Stream mode

FIFO Data

The latest frame stored in FIFO is identical to the data in the read-out PRESS_DATA[23:0] and TEMP_DATA[23:0].Thus, all configuration settings apply to the FIFO frame as well as the data readout registers. The readout can be performed using burst mode since the read address counter is no longer incremented, when the burst read access starts below address

FIFO_DATA (0x14). A single burst is recommended to read out one or more frames at a time.

FIFO_PRESS_EN bit and FIFO_TEMP_EN bit in register FIFO_CONFIG_0 (0x19) controls the storage of pressure or temperature measurements in the FIFO, respectively. If both pressure and temperature are enabled, the format of the data read-out from register FIFO_DATA (0x14) is as follows:

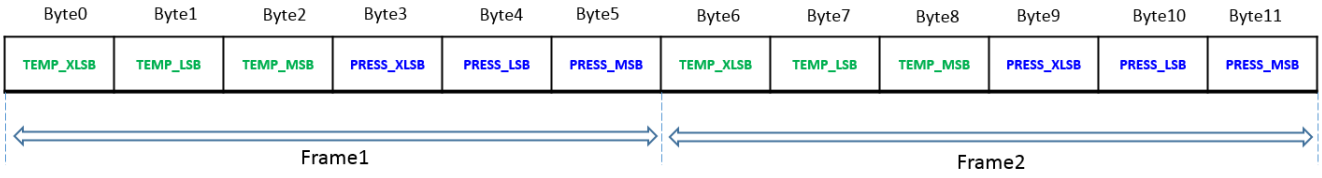


Figure 13: Frame format when both pressure and temperature are enabled

If only pressure or temperature is enabled, the format of the data read-out from register FIFO_DATA (0x14) is as follows: (Example shown pressure only, temperature is equivalent)

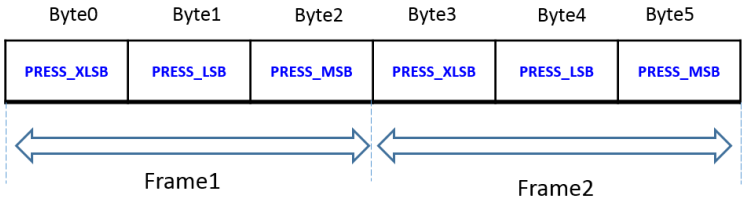


Figure 14: Frame format when only pressure is enabled

Moreover, FIFO_SUBSAMPLING[2:0] controls the data storage interval, and users can select the subsampling frequency in $2^{FIFO_SUBSAMPLING[2:0]}$samples that the data will be automatically stored into FIFO.

FIFO_BYTE_CNT[9:0] in register FIFO_LENGTH_0/1 (0x12/0x13) indicates the number of bytes available in the buffer. The FIFO byte count registers is only updated when an entire frame has been stored into the buffer and is ready to be read. The FIFO byte count register is also updated every time an entire frame is read from the FIFO. When the user issues a FIFO flush or software reset command in register RESET(0x7E), both FIFO buffer and FIFO_BYTE_CNT[9:0] are reset.

Partial frame read

To be sure the data integrity, a frame shall be the minimum unit (6 bytes for pressure and temperature, or 3 bytes for pressure or temperature only) for FIFO reading. If a frame is not properly read due to an incomplete read operation, the entire last data frame is repeated on the next read access.

In stream mode, if FIFO is full, the oldest frame will be overwritten when new frames are ready. In the case, the partially read data frame is discarded but replace by the oldest frame available in the buffer.

5.4 Interrupts

Interrupt Pin Output Types

The output mode can be set as Push-Pull or Open-Drain via the INT_OD bit, and the active level can be configured as active-high or active-low via the INT_LV bit. However, the status bits are not affected by this.

Data Ready Interrupt

The data ready interrupt serves for synchronous reading of sensor data. It is generated after storing a new value of pressure or temperature data in the data register. The interrupt is cleared automatically when the next cycle of data acquisition starts. The interrupt mode of data ready interrupt is kept to non-latched for about 200μs.

Address	Control Register	Bit	Bit Name	Function
03h	Status	[5] [6]	DRDY_PRESS DRDY_TEMP	Data ready for pressure and temperature. It gets reset, when PRESS_DATA[23:0] and TEMP_DATA[23:0]is read out.
11h	INT_STATUS	[4]	DRDY_INT	Data ready interrupt status. Synchronized with INT pin.
19h	INT_CTRL	[6]	DRDY_EN	Data ready interrupt enable bit. '1': enabled, '0': disabled.

FIFO Interrupts

The FIFO controller can generate two different interrupt events, a FIFO-full and a watermark event. The FIFO-full and watermark interrupts are both available in all FIFO operating modes.

To enable the FIFO watermark interrupt, the FWTM_EN bit in register INT_CTRL (0x19) must be set to '1' that routes the interrupt signal to INT pin. The watermark interrupt is asserted when the bytes level in the buffer reaches the level defined by FIFO_WM[9:0] in register FIFO_WM_0/1 (0x15/0x16). Meanwhile, the status of the watermark interrupt can be read back via FWM_INT bit in register INT_STATUS (0x11).

To enable the FIFO-full interrupt, the FFULL_EN bit in register INT_CTRL (0x19) must be set to '1'. The FIFO-full interrupt is triggered when the buffer has been fully occupied and that means 576 bytes in the FIFO buffer. The status of the FIFO-full interrupt is also displayed in the FFULL_INT bit in register INT_STATUS (0x11).The latch type of FIFO interrupt can be set as level type or pulse type via FIFO_INT_TYPE bit in register INT_CTRL (0x19).

Address	Control Register	Bit	Bit Name	Function
11h	INT_STATUS	[0] [1]	FWM_INT FFULL_INT	Data ready interrupt status. Synchronized with INT pin.
15h 16h	FIFO_WM_0 FIFO_WM_1	[7:0] [1:0]	FIFO_WM[9:0]	FIFO watermark level configuration.
19h	INT_CTRL	[4] [5]	FWTM_EN FFULL_EN	FIFO watermark and FIFO-full enable bit. '1': enabled, '0': disabled.
		[7]	FIFO_INT_TYPE	'1': pulse type, '0': level type.

5.5 User Register Map

Table 4: User Register Map Table

Addr.	Name	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Access	Default

00h	CHIP_ID	CHIP_ID[7:0]							R	0xA0
01h	REV_ID	REV_ID[7:0]							R	0x80
02h	ERR_MSG						CONF_ERR		R	0x00
03h	STATUS		DRDY_TEMP	DRDY_PRESS						0x00
04h	PRESS_XLSB	Pressure Data [7:0]							R	NA
05h	PRESS_LSB	Pressure Data[15:8]							R	NA
06h	PRESS_MSB	Pressure Data[23:16]							R	NA
07h	TEMP_XLSB	Temperature Data[7:0]							R	NA
08h	TEMP_LSB	Temperature Data[15:8]							R	NA
09h	TEMP_MSB	Temperature Data[23:16]							R	NA
0Ch	SENSOR_TIME_0	SENSOR_TIME[7:0]								0x00
0Dh	SENSOR_TIME_1	SENSOR_TIME[15:8]								0x00
0Eh	SENSOR_TIME_2	SENSOR_TIME[23:16]								0x00
11h	INT_STATUS				DRDY_INT			FFULL_INT	FWM_INT	0x00
12h	FIFO_LENGTH_0	FIFO_BYTE_CNT[7:0]								0x00
13h	FIFO_LENGTH_1							FIFO_BYTE_CNT[9:8]		0x00
14h	FIFO_DATA	FIFO_DATA[7:0]								0x00
15h	FIFO_WM_0	FIFO_WM[7:0]								0x01
16h	FIFO_WM_1							FIFO_WM[9:8]		0x00
17h	FIFO_CONFIG_0				FIFO_TEMP_EN	FIFO_PRESS_EN		FIFO_MODE	FIFO_EN	0x1A
18h	FIFO_CONFIG_1					DATA_SEL	FIFO_SUBSAMPLING[2:0]			0x02
19h	INT_CTRL	FIFO_INT_TYPE	DRDY_EN		FFULL_EN	FWTM_EN		INT_LV	INT_OD	0x02
1Ah	IF_CONFIG						I2C_WDT_SEL	I2C_WDT_EN	SPI3_EN	0x00

1Bh	PWR_CTRL			PWR_MODE[1:0]			TEMP_EN	PRESS_EN			0x00
1Ch	OSR		OSR_T[2:0]			OSR_P[2:0]					0x00
1Dh	ODR				ODR_SEL[4:0]						0x00
1Fh	FILTER		IIR_COEF_T[2:0]			IIR_COEF_P[2:0]					0x00
7Eh	RESET	RESET_CMD[7:0]									0x00
50h ~ 69h	Calib00 ~ Calib17	Calibration data								R	NA

5.6 Description of Registers

Register 00h: Chip_ID Register

Addr.	Name	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Access	Default
00h	CHIP_ID	CHIP_ID[7:0]								RW	0xA0

The register contains the chip identification code,0XA0.

Register 01h: Rev_ID Register

Addr.	Name	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Access	Default
01h	Rev_ID	REV_ID[7:0]								RW	0x80

The register contains the chip revision code,0X80.

Register 02h: ERR_MSG Register

Addr.	Name	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Access	Default
02h	ERR_MSG						CONF_ERR			R	0x00

The CONF_ERR indicates a setup error between ODR and OSR. Latched to '1' if an error occurred and cleared to '0' after reading.

Register 03h: Status Register

Addr.	Name	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Access	Default

03h	Status		DRDY_TEMP	DRDY_PRESS						R	0x00

The DRDY_PRESS bit is the data ready flag for pressure data. Latched to '1' if new data is ready and cleared to '0' after reading.

The DRDY_TEMP bit is the data ready flag for temperature data. Latched to '1' if new data is ready and cleared to '0' after reading.

Register 04h~06h: Pressure Data Registers

Addr.	Name	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Access	Default
04h	PRESS_XLSB	Pressure Data [7:0]								R	NA
05h	PRESS_LSB	Pressure Data [15:8]								R	NA
06h	PRESS_MSB	Pressure Data [23:16]								R	NA

The pressure data output is encoded to a 24-bit value and stored across three bytes. Data representation is 2's complement, i.e. MSB (bit 23) is the sign bit with 1'b1 representing negative value.

The pressure data output has sensitivity of 64LSB/Pa. The pressure value can be converted from the pressure reading by the following conversions:

$$\mathrm{P}(Pa) = \frac{Pressure\ Data[23:0]}{64}$$

Register 07h~09h: Temperature Data Registers

Addr.	Name	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Access	Default
07h	TEMP_XLSB	Temperature Data [7:0]								R	NA
08h	TEMP_LSB	Temperature Data[15:8]								R	NA
09h	TEMP_MSB	Temperature Data[23:16]								R	NA

The temperature data output is encoded to a 24-bit value and stored across three bytes. Data representation is 2's complement, i.e. MSB (bit 23) is the sign bit with 1'b1 representing negative value.

The temperature data output has sensitivity of 65536LSB/˚C. The temperature value can be converted from the temperature reading by the following conversions:

$$T(℃) = \frac{Temperature\ Data[23:0]}{65536}$$

Register 0Ch~0Eh: Sensor Time Registers

Addr.	Name	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Access	Default
0Ch	SENSOR_TIME_0	Sensor time[7:0]								R	NA
0Dh	SENSOR_TIME_1	Sensor time[15:8]								R	NA
0Eh	SENSOR_TIME_2	Sensor time[23:16]								R	NA

The sensor time data output is encoded to a 24-bit value and stored across three bytes.

Register 11h: INT_Status Register

Addr.	Name	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Access	Default
11h	INT_Status				DRDY_INT			FFULL_INT	FWM_INT	R	0x00

The register contains the interrupt status flags. External interrupt pin is synchronized with interrupt status flags.

The DRDY_INT bit : New data interrupt status. ‘1’ : event triggered, ‘0’ : no event.

The FFULL_INT bit : FIFO full interrupt status. ‘1’ : event triggered, ‘0’ : no event.

The FWM_INT bit: FIFO watermark interrupt status. ‘1’ : event triggered, ‘0’ : no event.

Register 12h~13h: FIFO_LENGTH Register

Addr.	Name	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Access	Default
12h	FIFO_LENGTH_0	FIFO_BYTE_CNT[7:0]								R	0x00
13h	FIFO_LENGTH_1							FIFO_BYTE_CNT[9:8]		R	0x00

FIFO_LENGTH_0 and FIFO_LENGTH_1 register contain the FIFO byte counter, which shows how many bytes of valid data are contained in the FIFO.

Register 14h: FIFO_DATA Register

Addr.	Name	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Access	Default
14h	FIFO_Data	FIFO_DATA[7:0]								R	0x00

This register contains FIFO data output. Burst read access may be used since the address counter will not increment when the burst read is started at the address of FIFO_DATA(14h). If the entire frame is not read out completely, the frame will be retained.

Data frame format depends on the setting of FIFO_PRESS_EN and FIFO_TEMP_EN. If both pressure data and temperature data are selected, the data of frame n is reading out in the order of TEMP_XLSB(n), TEMP_LSB(n),TEMP_MSB(n), PRESS_XLSB(n), PRESS_LSB(n), PRESS_MSB(n); if only pressure data is selected, the data of frame n and n+1 are reading out in the order of PRESS_XLSB(n), PRESS_LSB(n), PRESS_MSB(n), PRESS_XLSB(n+1),PRESS_LSB(n+1), PRESS_MSB(n+1); the temperature-only data mode behave analogously.

Data type	Byte Sequence	Content
Temperature	1	Temp_XLSB
	2	Temp_LSB
	3	Temp_MSB
Pressure	1	Press_XLSB
	2	Press_LSB
	3	Press_MSB

Register 15-16h: FIFO_WM_0/ FIFO_WM_1 Register

Addr.	Name	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Access	Default
15h	FIFO_WM_0	FIFO_WM[7:0]								R/W	0x01
16h	FIFO_WM_1							FIFO_WM[9:8]		R/W	

FIFO_WM_0 and FIFO_WM_1 register contains FIFO watermark level. If the number of unread bytes in the FIFO is equal to FIFO watermark level, an interrupt will be triggered. If ‘0’, the FIFO watermark interrupt is disabled.

Register 17h: FIFO_CONFIG_0 Register

Addr.	Name	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Access	Default

17h	FIFO_CONFIG_0				FIFO_TEMP_EN	FIFO_PRESS_EN		FIFO_MODE	FIFO_EN	R/W	

FIFO_CONFIG_0 register is used to configure the FIFO.

BIT	BIT NAME	Default Setting	Description
0	FIFO_EN	0	FIFO enable configuration. 0: Bypass Mode. 1: FIFO Mode
1	FIFO_MODE	1	FIFO mode configuration. Active when FIFO_EN = '1'. 0: FIFO stream mode. When the FIFO is full, NEW data will be preserved. 1: FIFO normal mode. When the FIFO is full, OLD data will be preserved.
3	FIFO_PRESS_EN	1	0: Do not store pressure data in FIFO. 1: Store pressure data in FIFO.
4	FIFO_TEMP_EN	1	0: Do not store temperature data in FIFO. 1: Store temperature data in FIFO.

Register 18h: FIFO_CONFIG_1 Register

Addr.	Name	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Access	Default
18h	FIFO_CONFIG_1					DATA_SEL	FIFO_SUBSAMPLING[2:0]			R/W	

FIFO_CONFIG_1 register is used to configure the FIFO.

BIT	BIT NAME	Default Setting	Description
[2:0]	FIFO_SUBSAMPLING	3'b010	FIFO data subsampling interval configuration. Subsampling interval is 2^FIFO_SUBSAMPLING
3	DATA_SEL	0	Data source selection. 0: Filtered data. 1: Unfiltered data. Bypass the settings in FILTER(1Fh).

Register 19h:INT_CTRL Register

Addr.	Name	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Access	Default
19h	INT_CTRL	FIFO_INT_TYPR	DRDY_EN		FFULL_EN	FWTM_EN		INT_LV	INT_OD	R/W	

INT_CTRL register contains INT pin output type and active level configuration, and several interrupts enable bit.

BIT	BIT NAME	Default Setting	Description
0	INT_OD	0	INT pin output type selection. 0: Push-pull output type. 1: Open-drain output type.
1	INT_LV	1	INT pin active level selection. 0: Active low. 1: Active high.
3	FWTM_EN	0	0: Disable FIFO watermark interrupt. 1: Enable FIFO watermark interrupt.
4	FFULL_EN	0	0: Disable FIFO full interrupt. 1: Enable FIFO full interrupt.
6	DRDY_EN	0	0: Disable data ready interrupt. 1: Enable data ready interrupt.
7	FIFO_INT_TYPE	0	0: FIFO interrupt is displayed as a latch type. 1: FIFO interrupt is displayed as a pulse type with a period of 50us.

Register 1Ah:IF_CONFIG_0 Register

Addr.	Name	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Access	Default
1Ah							I2C_WDT_SEL	I2C_WDT_EN	SPI3_EN	R/W	

The 1Ah register contains interface configuration for I2C and SPI.

BIT	BIT NAME	Default Setting	Description
0	SPI3_EN	0	SPI 3-wire interface activation. 0: 4-wire SPI interface used. 1: 3-wire SPI interface used.
1	I2C_WDT_EN	0	I2C watchdog timer enable bit. 0: Disable I2C watchdog timer. 1: Enable I2C watchdog timer.
2	I2C_WDT_SEL	0	I2C watchdog timer period selection. 0: Watchdog timer period 1ms. 1: Watchdog timer period 50ms.

Register 1Bh:PWR_CTRL Register

Addr.	Name	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Access	Default
1Bh				POWER_MODE [1:0]				TEMP_EN	PTESS_EN	R/W	

The 1Bh register contains sensor switch and power mode configuration.

BIT	BIT NAME	Default Setting	Description
0	PRESS_EN	0	0: Disables the pressure sensor. 1: Enables the pressure sensor.
1	TEMP_EN	0	0: Disables the temperature sensor. 1: Enables the temperature sensor.
[5:4]	PWR_MODE	2'b00	Power mode configuration.. 2'b00: Sleep. 2'b01:Florced mode 2'b10:Reserve 2'b11:Normal Mode

Register 1Ch:OSR Register

Addr.	Name	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Access	Default
1Ch			OSR_T				OSR_P			R/W	

The 1Ch register is used to configure oversampling ratio for pressure and temperature measurement.

BIT	BIT NAME	Default Setting	Description
[2:0]	OSR_P	3'b000	Oversampling ratio for pressure measurement. 3'b000 x1 3'b001 x2 3'b010 x4 3'b011 x8 3'b100 x16 3'b101 x32 3'b110 x64 3'b111 x128
[6:4]	OSR_T	3'b000	Oversampling ratio for temperature measurement. 3'b000 x1 3'b001 x2

3'b010 x4 3'b011 x8 3'b100 x16 3'b101 x32 3'b110 x64 3'b111 x128

Pressure RMS Noise at different OSR setting, test at VDD=1.8V

Oversampling ratio	OSR Register 0x1C	RMS-Noise (Pa)
x1	0x00	9.0
x2	0x11	6.5
x4	0x22	4.5
x8	0x33	3.3
x16	0x44	2.6
x32	0x55	2.3
x64	0x66	2.0
x128	0x77	1.8

Register 1Dh:ODR Register

Addr.	Name	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Access	Default
1Dh	ODR				ODR_SEL[4:0]					R/W	

The 1Dh register is used to configure output data rate.

ODR_SEL[4:0] (Binary)	ODR_SEL[4:0] (HEX)	ODR (Hz)	Sampling Period(ms)
5'b00000	0x0	250	4
5'b00001	0x1	222	4.5
5'b00010	0x2	200	5
5'b00011	0x3	180	5.556
5'b00100	0x4	160	6.25
5'b00101	0x5	142.86	7
5'b00110	0x6	125	8
5'b00111	0x7	111	9
5'b01000	0x8	100	10
5'b01001	0x9	90	11.1
5'b01010	0xA	80	12.5

5'b01011	0xB	70	14.286
5'b01100	0xC	62.5	16
5'b01101	0xD	50	20
5'b01110	0xE	40	25
5'b01111	0xF	32	31.25
5'b10000	0x10	25	40
5'b10001	0x11	20	50
5'b10010	0x12	16	62.5
5'b10011	0x13	12.5	80
5'b10100	0x14	10	100
5'b10101	0x15	8	125
5'b10110	0x16	6.4	156.25
5'b10111	0x17	5	200
5'b11000	0x18	4	250
5'b11001	0x19	3.2	312.5
5'b11010	0x1A	2.5	400
5'b11011	0x1B	2	500
5'b11100	0x1C	1	1000
5'b11101	0x1D	0.5	2000
5'b11110	0x1E	0.25	4000
5'b11111	0x1F	0.125	8000

OSR and ODR Setting Suggestion

OSR Register 0x1C	Oversampling ratio	ODR Setting	Conversion Frequency (Hz)
0x00	x1	0x00	250Hz
0x11	x2	0x00	250Hz
0x22	x4	0x03	180Hz
0x33	x8	0x08	100Hz
0x44	x16	0x0D	50Hz
0x55	x32	0x10	25Hz
0x66	x64	0x13	12.5Hz
0x77	x128	0x16	6.4Hz

Register 1Fh:FILTER Register

Addr.	Name	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Access	Default
1Fh	FILTER		IIR_COEF_T				IIR_COEF_P			R/W	

The 1Fh register is used to configure the IIR filter coefficients for pressure and temperature measurement.

IIR_COEF_P	Filter Coefficients
3'b000	0
3'b001	1
3'b010	3
3'b011	7
3'b100	15
3'b101	31
3'b110	63
3'b111	127

IIR_COEF_T	Filter Coefficients
3'b000	0
3'b001	1
3'b010	3
3'b011	7
3'b100	15
3'b101	31
3'b110	63
3'b111	127

Pressure RMS Noise, at different IIR setting, test at VDD=1.8V

IIR_COEF_P/T	Filter Coefficients	OSR Register Setting	OSR-P	OSR-T	ODR Register Setting	Conversion Frequency (Hz)	RMS Noise,Pa
3'b000	0	0x77	X128	X128	0x16	6.4Hz	1.8
3'b001	1	0x77	X128	X128	0x16	6.4Hz	1.6
3'b010	3	0x77	X128	X128	0x16	6.4Hz	1.4
3'b011	7	0x77	X128	X128	0x16	6.4Hz	0.8
3'b100	15	0x77	X128	X128	0x16	6.4Hz	0.5
3'b101	31	0x77	X128	X128	0x16	6.4Hz	0.2
3'b110	63	0x77	X128	X128	0x16	6.4Hz	0.1

3'b111	127	0x77	X128	X128	0x16	6.4Hz	0.1

Register 7Eh: RESET Register

Addr.	Name	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Access	Default
7Eh	RESET	RESET_CMD[7:0]								W	0x00

The 7Eh register is used to reset command.

RESET_CMD[7:0]	Name	Description
0XB0	FIFO_flush	Clear all data in the FIFO, but keep FIFO settings.
0XB6	Software reset	Reset all registers to default value, and set IC to default state.

6. DIGITAL INTERFACE

6.1 I2C Interface

I2C Interface General Description

The I2C interface is compliant with standard and fast I2C standard. The devices support the 7-bit control functions and SDA and SCL facilitate communication between QMP6990 and master with clock rate up to 400kHz.

The 7-bit device slave address can be selected by the SA0 pin as summarized in the below table.

SA0	7-bit Slave Address
1'b0	0x3A
1'b1	0x3B

I2C Specifications

Slave Address

CS pin	SA0 pin	Slave Address (7-bit)	R/W Command Bit	OPERATION
1 or float	0	0X3A	0	Write Data to ASIC
			1	Read Data form ASIC
	1	0X3B	0	Write Data to ASIC
			1	Read Data form ASIC

Figure 13: I2C START and STOP condition

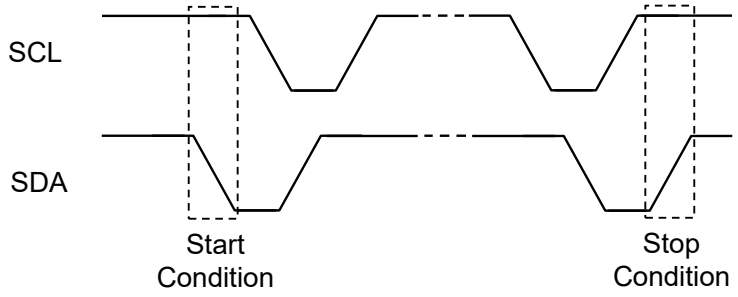


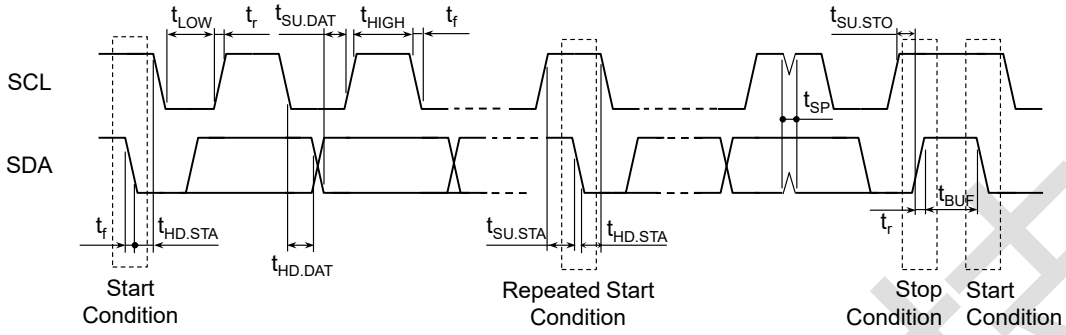
Table 5: I2C Timing Specification: Standard Mode

Parameter	Symbol	Minimum	Typical	Maximum	Unit
SCL clock frequency	f_{SCL}	—	—	100	kHz
Clock low period	t_{LOW}	4.7	—	—	μs
Clock high period	t_{HIGH}	4	—	—	μs
Start hold time	$t_{HD.STA}$	4	—	—	μs
Start setup time	$t_{SU.STA}$	4.7	—	—	μs
Data-in hold time	$t_{HD.DAT}$	0	—	—	μs
Data-in setup time	$t_{SU.DAT}$	250	—	—	ns
Stop setup time	$t_{SU.STO}$	4	—	—	μs
Rise time	t_r	—	—	1	μs
Fall time	t_f	—	—	0.3	μs

Table 6: I2C Timing Specification: Fast Mode

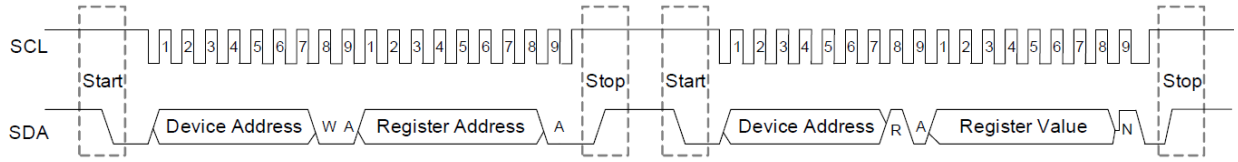
Parameter	Symbol	Minimum	Typical	Maximum	Unit
SCL clock frequency	f_{SCL}	—	—	400	kHz
Clock low period	t_{LOW}	1.3	—	—	μs
Clock high period	t_{HIGH}	0.6	—	—	μs
Bus free to new start	t_{BUF}	1.3	—	—	μs
Start hold time	$t_{HD.STA}$	0.6	—	—	μs
Start setup time	$t_{SU.STA}$	0.6	—	—	μs
Data-in hold time	$t_{HD.DAT}$	0	—	—	μs
Data-in setup time	$t_{SU.DAT}$	100	—	—	ns
Stop setup time	$t_{SU.STO}$	0.6	—	—	μs
Rise time	t_r	—	—	0.3	μs
Fall time	t_f	—	—	0.3	μs
Spike width	t_{SP}	—	—	50	μs

Timing Chart of the I2C

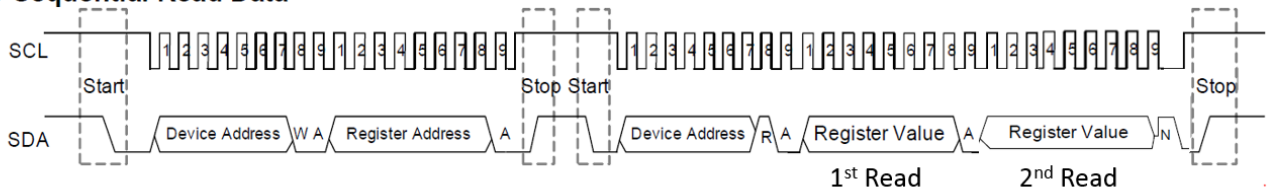


I²C Write Command

I²C Read Data



I²C Sequential Read Data



6.2 SPI Interface

The QMP6990 is also compatible with ‘00’ (mode 0) and ‘11’ (mode 3) SPI mode. The automatic selection between ‘00’[CPOL = 0 and CPHA = 0] and ‘11’ [CPOL = 1 and CPHA = 1] is done based on the SCK value at the falling edge of /CS.

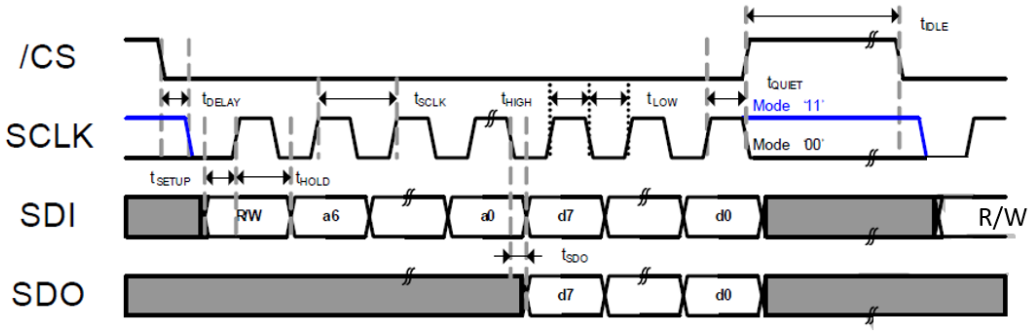
The 3-or 4-wire SPI connection diagram are shown below. The maximum SPI clock speed is 10MHz with 25pF maximum loading. The 3-wire SPI can be selected by setting SPI3_EN bit in IF_CONFIG (0x1A) to 1. When using 3-wire SPI, it is recommended that the SDO pin either be pulled up to VDDIO or be pulled down to GND via a 10 kΩ resistor.

Table 7: SPI Timing Specification

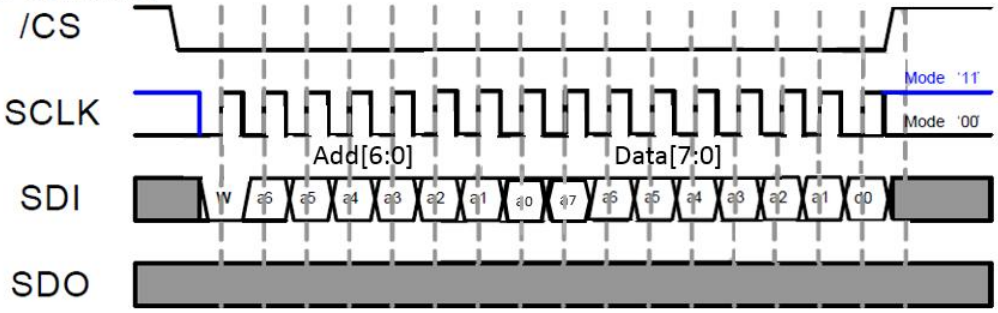
Parameter	Symbol	Condition	Minimum	Maximum	Unit
SPI clock frequency.	F_{SCK}			10	MHz
1/ f_{SCLK}	t_{SCKL}		125	—	ns
SCLK high pulse width.	t_{HIGH}		62.5	—	ns
SCLK low pulse width.	t_{LOW}		62.5	—	ns
/CS falling edge to SCLK falling edge.	t_{DELAY}		30	—	ns
SCLK rising edge to /CS rising edge	t_{QUITE}		70	—	ns
Set-up time for SDI	t_{SETUP}		20	—	ns
Hold time for SDI	t_{HOLD}		20	—	ns
SDO output delay	t_{SDO}	VDDIO > 2.2V		30	ns
		VDDIO ≤ 2.2V		40	ns
SPI bus idle time between two success bus transactions	t_{IDLE}		20		ns

Figure 14: SPI Timing Diagram

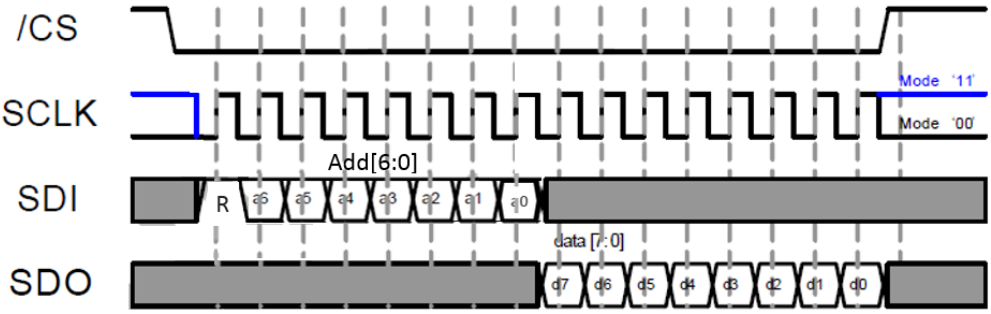
Timing Chart of the SPI



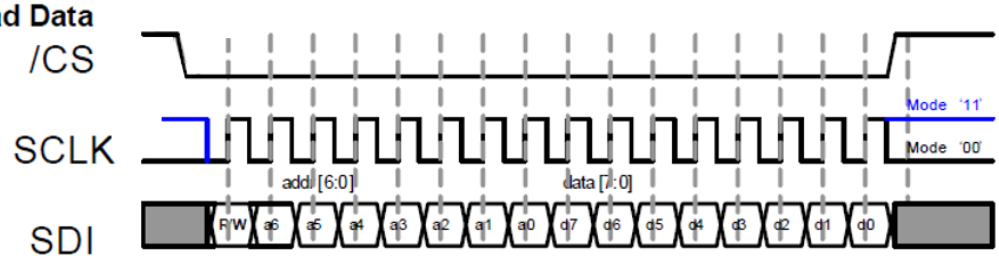
SPI 4-Wire Write Command



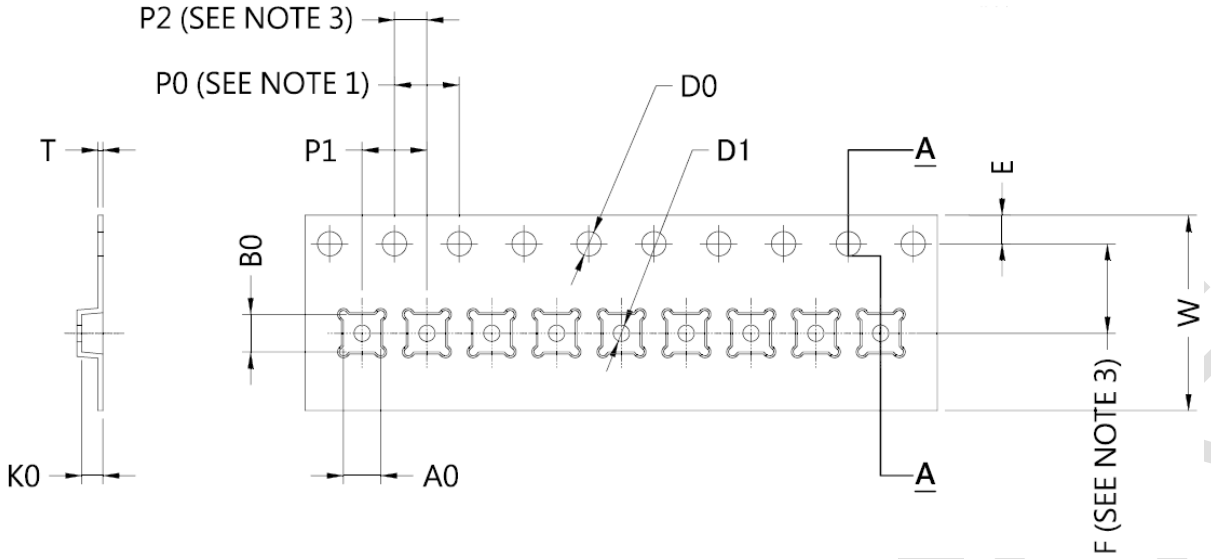
SPI 4-Wire Read Data



SPI 3-Wire Read Data



7. TAPE AND REEL SPECIFICATION



Item	Specification	Tol. (+/-)	Item	Specification	Tol. (+/-)
W	12.00	±0.30	A0	2.30	±0.10
E	1.75	±0.10	B0	2.30	±0.10
F	5.50	±0.05	K0	1.30	±0.10
D0	1.50	+0.1/-0.0	T	0.30	±0.05
D1	1.00	MIN			
P0	4.00	±0.10			
P1	4.00	±0.10			
P2	2.00	±0.05			

Notes:

1. 10 sprocket hole pitch cumulative tolerance ±0.2
2. Camber in compliance with EIA 481
3. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole

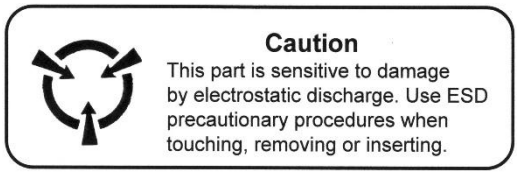
Packing Information

ITEM	Packing information
1	Pizza box (inner box) : Size=36x34x4cm 1 REEL= 5K
2	Carton (Outter box) : Size=37.5*28.5*36cm 1 Carton= 7 REEL = 35K

Pin 1 orientation

Orientation type	A	B	C	D
Orientation in carrier				

ORDERING INFORMATION



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REVISION RECORD

Rev.	Date	Originator	Change Description
V0.1	2024/10/14		First release
V0.2	2025/1/15		Update pressure, temperature resolution description and carrier dimension